IN THE UNITED STATES OF AMERICA

PATENT AND TRADEMARK OFFICE

APPLICANT:	PEIYI ZHAO TAREK DARWISH MADGY BAYOUMI	SERIAL NO.: 10/628,737
TITLE:	SINGLE-TRANSISTER-CLOCKED FLIP-FLOP	
DOCKET NO.:	17220-6	
FILING DATE:	July 28, 2003	

MAIL STOP PATENT APPLICATION
COMMISSIONER FOR PATENTS
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IN THE UNITED STATES OF AMERICA

PATENT AND TRADEMARK OFFICE

APPLICANT(S): PEIYI ZHAO
TAREK DARWISH
MADGY BAYOUMI

TITLE: SINGLE-TRANSISTER-CLOCKED FLIP-FLOP

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INFORMATION DISCLOSURE STATEMENT

The following information is submitted pursuant to 37 CFR § 1.97 et seq.

Applicant, through his attorney, submits Form PTO/SB/08A, which is attached. The patents, publications or other information listed on the attached form are those of which he is aware, which he believes may be material to the examination of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR § 1.56.

The filing of this information disclosure statement shall not be construed as a representation that a search has been made (37 § C.F.R. 1.97(g)), an admission that the information cited is, or is considered to be, material to patentability, or that no other material information exists.

The filing of this information disclosure statement shall not be construed as an admission against interest in any manner.

This information is based upon information supplied by the inventor and information in the attorney's file.

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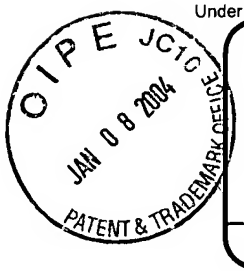

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 1

Compl te if Known	
Application Number	10/628,737
Filing Date	July 28, 2003
First Named Inventor	PEIYI ZHAO
Group Art Unit	Not Assigned
Examiner Name	Not Assigned
Attorney Docket Number	17220-6

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (*if known*)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	5,453,708		Gupta et al.	09-26-1995	
	2	5,557,225		Denham et al.	09-17-1996	
	3	5,764,089		Partovi et al.	06-09-1998	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (*if known*)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

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Sheet 1 of 1

Complet if Known	
Application Number	10/628,737
Filing Date	July 28, 2003
First Named Inventor	PEIYI ZHAO
Group Art Unit	Not Assigned
Examiner Name	Not Assigned
Attorney Docket Number	17220-6

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	1	SEONGMOO HEO, RONNY KRASHINSKY, AND KRSTE ASANOVIE, Activity-Sensitive Flip-Flop and Latch Selection for Reduced Energy, 19th Conference on Advanced Research in VLS1, Salt Lake City, UT, March 2001	
	2	HIROSHI KAWAGUCHI and TAKAYASU SAKURAI, A Reduced Clock-Swing Flip-Flop (RCSFF) for 63% Power Reduction, IEEE Journal of Solid-State Circuits, Vol. 33, No. 5, May 1998.	
	3	SEONGMOO HEO and KRSTE ASANOVIE, Load-Sensitive Flip-Flop Characterization, IEEE Journal of Solid-State Circuits, 2001	
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	5	JIREN YUAN and CHRISTER SVENSSON, High-Speed CMOS Circuit Technique, IEEE Journal of Solid-State Circuits, Vol. 24, No. 1, February 1989.	
	6	RABAEY, J.M.: Digital Integrated Circuits, Chapter 7, "Designing Sequential Logic Circuits", University of California, Berkeley, 2000,	
	7	VLADIMIR STOJANOVIC and VOJIN G. OKLOBDZIJA, Comparative Analysis of Master-Slave Latches and Flip-Flops for High-Performance and Low-Power Systems, IEEE Journal of Solid-State Circuits, Vol.34, No. 4, April 1999.	
	8	J. TSCHANZ, etal., Comparative Delay and Energy of Sgl. Edge-Triggered & Dual Edge-Triggered Pulsed Flip-Flops for Hi-Performance Microprocessors Intn'l Symp. on Low Power Elect and Design, Pp(s): 147-152, 2001.	

Examiner Signature		Date Considered	

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